JL6110 Product Brief

10 Port Lite-Management Gigabit Ethernet Switch

JLSemi Limited

PB014-JL6110-v1.00-EN

JLSemi

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Overview

The JL6110 is a 10-port high-performance Gigabit Ethernet switch with two RGMII/MII/RMII or 1000BASE-X/100BASE-FX/H-SGMII/SGMII. The switch is highly integrated and smartmanaged with 8 GE PHY and RISC-V inside. The device also combines rich functions of standard GE switch system, including packet buffers, address management, VLAN, ACL, QoS, MIB, etc.

The JL6110 contains eight full-duplex 10/100/1000 Mb/s Ethernet transceivers. In addition, the device has two PHY-less interfaces for the external CPU or external PHY chip, providing flexible 10/100/1000/2500 Mb/s connectivity. The two mac interface ports can also be connected to optical modules with 100Base-FX, 1000Base-X, or 2500Base-X ports.

The JL6110 also integrates a powerful RISC-V CPU system to support smart management, such as web-smart function and cloud management. In addition, the JL6110 also supports RTOS to run upper-layer software protocols.

Typical Applications

- 8-port to 10-port Lite-Managed Gigabit Switch or Dump Switch
- 8-port Router
- Ethernet bridge module

Features

- Ten 10/100/1000 Media Access Controllers (MAC)
- 8-port 10/100/1000BASE-T transceivers
- Two interfaces support RGMII/MII/RMII, SGMII/2500BASE-X/1000BASE-X/100BASE-FX
- Each port supports full-duplex 10/100/1000M connectivity (half duplex only supported in 10/100M mode)
- Full-duplex and half-duplex operation with IEEE 802.3x flow control and backpressure
- Embedded RISC-V up to 156.25 MHz
- Basic Switching Function

 Non-blocking wire-speed reception and transmission and non-HOL forwarding
 - Supports L2 switching, 4K L2 Mac table entry, aging time range 2s to 1600s, software accessible
 - $\circ~$ Jumbo Frame size: 16 KB
 - $\circ~$ Supports full mesh test from 64B to 1518B
 - Supports Broadcast/Multicast/Unknown DA storm control to protect system from attack by hackers
 - Supports one set of port mirroring functions for all ports. The TX, or RX, or both TX/RX packets of the source port can be monitored from a mirror port.



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Features

- ACL feature
 - Supports 128-entry ACL rules

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- Search key supports physical port, layer2, layer3, and layer4 information
- Each port can optionally enable or disable the ACL rule check function
- Actions support permit, mirror, redirect, dropping, priority adjustment, traffic policing, and VLAN update.
- $\circ~$ Supports types of user-defined ACL rule format
- VLAN feature
 - \circ Supports port-based VLAN
 - $\circ~$ Supports IEEE802.1Q-based VLAN with 4096 entries
 - Supports VLAN policing and VLAN forwarding decision
 - Supports per-port and per-VLAN egress VLAN tagging and un-tagging
 - $\circ~$ Supports Egress VID modification
 - Supports double-tagging
- STP feature
 - IEEEE 802.1D STP
 - IEEEE 802.1w Rapid Spanning Tree
 - IEEE 802.1s Multiple Spanning Tree up to 16 Spanning Tree instances
- QoS feature
 - \circ 8 priority queues per port
 - Traffic classification based on IEEE 802.1p/Q priority definition, physical Port, IP DSCP field, ACL definition, VLAN based priority, MAC based priority, and SVLAN based priority

- Strict Priority and DWRR to provide a minimum bandwidth
- Priority modification on egress
- Supports rate limiting based on Port/Queue/ Priority
- Other features

 Support trunk function
 - RFC MIB Counter
 - Security filtering: Disable learning for each port.
 Disable learning-table aging for each port.
 Drop unknown DA for each port
 - Supports IEEEE 802.3 reserved group address filtering control
 - Supports IGMP v1/v2/v3 and MLD v1/v2 snooping. Trap all IGMP and MLD packets to the CPU port.
 - Supports SPI Flash interface
 - Supports SMI/I2C/SPI management interface to access configuration register
 - Each port supports 3 parallel LED or serial LED or scan LED outputs
 - $\circ~$ 25 MHz crystal input
 - TQFP 176-pin EPAD package